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An integrated and intelligent DSS for manufacturing systems

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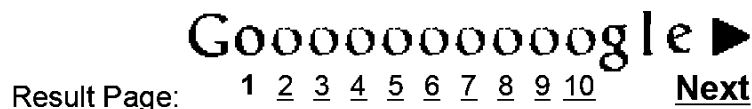
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... that FMS **analysis** is inappropriate for **PCB** assembly system **analysis**: FMS **analysis** chooses
among ... In **PCB** assembly, however, the production cycle is fixed (eg, receiving inspection, panel
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 ... SPICE is a mature circuit **simulation** tool with many well-developed IC, source, load, and transmission ... The data replotted in this format is particularly useful for **interpolating** the board thickness ... In practical designs, the number of **PCB** layers and layer stackup that dictates power ...

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KN Chiang, CM Liu - ... in Electronic Systems, 2000. ITherm 2000. ..., 2000 - csml9.pme.nthu.edu.tw
 ... level packaging, fine pitch BGA (ball grid array) and high density interconnects, the wireability of the **PCB**/substrate and ... Moreover, two SBM **simulation** models (analytical and energy-based methods) that described in the previous section may be ... restoring force **interpolation**. ...

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HJ Albrecht, DC Hyslop, J Jendreny, WH ... - IEEE, 2000 ..., 2000 - [mechanik.tu-berlin.de](#)

... It should be noted that due to the numerical **interpolation** of the sub-model boundary conditions from the global model, a ... **PCB** Board 45µm ... References 1. Dudek, R., Scherzer, M., Schubert, A., Michel, B., "FE- **Simulation** for Polymeric Packaging Materials," IEEE Transactions on ...

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JR Culham, TF Lemczyk, S Lee, MM ... - Proceedings of the 1991 ..., 1991 - [mhtl.uwaterloo.ca](#)

... It is to this end that META (Mcro£lectronic Hhermal Analyser), the **simulation** routine presented in ... across the **PCB** using this ap- proximation, it was shown that the **PCB** thermal resistance ... of the delay function on the type of convective heat transfer, an **interpolation** between the ...

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S Goumas, GA Rovithakis, M ... - Image Processing. ..., 2002 - [www-video.eecs.berkeley.edu](#)

... Surface **Mount** technology Devices (SMDs) are in this direction, thus explaining the substantial increase ... placement, so no extra time and components are spent on an already faulty **PCB**. ... For designing and training the classifiers we employ the Monte Carlo **simulation** process, in ...

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W Zhiping, N Jingxu - ACTA MECHANICA SINICA (English Series), 2002 - cstam.org.cn

... **PCB PCB** BT BT ... It was found that the results from the numerical **simulation** are in good agreement with the results from the MDS tests, either by the type of failure site or fatigue life. ...**Solder** joint reliability of fine pitch surface **mount** technology assemblies. ...Cited by 6 - [Related articles](#) - [View as HTML](#) - [All 2 versions](#)**A profile identification system for surface mount printed circuit board assembly**

YY Su, K Srihari, CR Emerson - Computers & industrial engineering, 1997 - Elsevier

... temperature, and the maximum temperature increase and decrease that the **PCB** and or ... The IR radiation forced convection oven temperature profile **simulation** generated by the ... Lea, C., (1988), A Scientific Guide To Surface **Mount** Technology, Electrochemical Publications, Ayr ...Cited by 9 - [Related articles](#) - [BL Direct](#) - [All 8 versions](#)**Critical factors affecting paste flow during the stencil printing of solder paste**R Durairaj, TA Nguty, NN Ekere - **Soldering** and Surface **Mount** ..., 2001 - emeraldinsight.com... stencil walls compete directly with the adhesives/pull force on the **PCB** pads, often ... EK (1994), "Mapping of manufacturing process modelling", **Soldering** and Surface **Mount** Technology Journal ... Mannan, SH, Ekere, NN, Ismail, I., Currie, MA (1994), "Computer **simulation** of solder ...Cited by 11 - [Related articles](#) - [BL Direct](#) - [All 6 versions](#)**... of solder paste rheology with computational simulations of the stencil printing ...**R Durairaj, GJ Jackson, NN Ekere, G ... - **Soldering** and Surface ..., 2002 - emeraldinsight.com... by computational **simulation**. This paper describes paste characterisation and computational **simulation** studies that ... is a critical stage in the mass production **assembly** of surface **mount** components. ... As **PCB** pad and component lead sizes continue to reduce, most paste suppliers ...Cited by 12 - [Related articles](#) - [BL Direct](#) - [All 5 versions](#)**... -based process planning system for the surface mount manufacture of PCBs**

K Srihari, JA Cecil, CR Emerson - The International Journal of Advanced ..., 1994 - Springer

... The outputs that are then formatted and provided to the user include: 1. The suggested sequence of surface **mount assembly** operations for a **PCB**. Page 6. ... The **simulation** would help to visualise the movement of the **PCBs**, the working of the **assembly** line, etc. ...Cited by 7 - [Related articles](#) - [BL Direct](#) - [All 3 versions](#)**Flow processes in solder paste during stencil printing for SMT assembly**

SH Mannan, NN Ekere, I Ismail, MA Currie - Journal of Materials Science: ..., 1995 - Springer

... 1. Introduction The use of surface **mount** technology (SMT) has grown rapidly in recent years, but ... After the paste has entered the apertures, the next crucial stage is stencil-**PCB** separation. ... It has been observed in a computer **simulation** [14] that a wider particle size distribution ...Cited by 8 - [Related articles](#) - [BL Direct](#)

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Neural network solder paste inspection system

SM Bryant, KH Loewenthal - US Patent 5,751,910, 1998 - Google Patents

... USING CRISP INPUT VECTOR APPLY BACK PROPAGATION TRAINING USING FUZZY OUTPUT VECTOR HAS ... Neural networks have also been used in imaging **mount** technology (SMT) components or ... paradigm, cally secured and electrically connected to the **PCB** by Neural ...Cited by 10 - [Related articles](#) - [All 4 versions](#)[BOOK] Spatial reasoning for effective GIS

JK Berry - 1996 - books.google.com

... E-mail: books@gisworld.com Edited by John Hughes Designed and composed by Wade Smith Project managed by Bea Ferrigno Second **Printing**. ... For example, a geographic distribution (3-D surface) of **PCB** concentra- tions in an aquifer can be **interpolated** from water ...Cited by 50 - [Related articles](#) - [All 5 versions](#)[PDF] •System implementation, modeling and defects pattern recognition for flip chip ...

S Liu - 2001 - me.gatech.edu

... It can also be extended to inspect solder bumps on BGAs, chip scales, MCMs, and other surface **mount** components in the future. ... The screen-**printing** process puts pastes of solders on ... After assembling the entire printed circuit board (**PCB**), the testing fixture checks for Page 26. ...[Related articles](#) - [View as HTML](#) - [All 5 versions](#)[BOOK] Computational intelligence in manufacturing handbook

J Wang, A Kusiak - 2001 - books.google.com

... It represents a union of neural networks, **fuzzy** systems, evolutionary computation techniques, and other emerging intelligent agents and technologies. ... Chapter 5 by Kazerooni et al. discusses an application of **fuzzy** logic to design flexible manufacturing systems. ...Cited by 10 - [Related articles](#) - [Library Search](#) - [All 2 versions](#)Devices and methods for optically identifying characteristics of material objects

I Wunderman, AE Smith, VK Lumba - US Patent 6,122,042, 2000 - Google Patents

... object surface. FIG. 2A is a cross-sectional view of a particular embodi- ment of an IDEA probe. FIG. 2B details the drive electronics of an LED **PCB**. FIG. 2C details the detector electronics 42 of a detector **PCB**. FIG. 2D shows ...Cited by 18 - [Related articles](#) - [All 2 versions](#)[BOOK] Junk science judo: Self-defense against health scares & scams

SJ Milloy - 2001 - books.google.com

... All right reserved. Second **printing**: March 2002 Library of Congress Cataloging-in-Publication Data Milloy, Steven J. Junk science judo : self-defense against health scares and scams / by Steven J. Milloy. ... Broadcast media care about ratings. **Print** media care about circu- lation. ...Cited by 15 - [Related articles](#)

A review of computer graphics publications

ID Benest - Computers & Graphics, 1979 - Elsevier

... graphics in computer circuit analysis 13.3 Printed circuit board layout at REDAC Software Limited
13.4 Surface plotter 13.5 PLOT 3D surface plotter 13.6 Surface **interpolation** 13.7 Polygon ... The
image so produced was used for **printing** by the standard photo- offset technique. ...

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•A data structure and query algorithm for a database of areal entities

DJ Abel, JL Smith - Australian Computer Journal, 1984 - acs.org.au

... The scheduling technique has provision for putting such jobs 'to one side' and for informing the
operators of tape **mounting** requirements, without holding up the ... Keywords = {Photocomposition,
Printing Industry, Text Composition ... Title = {A Stable Method of Inverse **Interpolation**},. ...


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[BOOK] Deep Descent: Adventure and Death Diving the Andrea Doria

KF McMurray - 2002 - books.google.com

... display. The Andrea Doria is often called the "**Mount** Everest of wreck div- ing," although
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Simulation software for surface **mount assembly**

TM Tirpak - ... of the 25th conference on Winter **simulation**, 1993 - portal.acm.org
 ... of the software, ie, the routines for managing input data, outputs, and process **models**. ... industry and typi- cally involves the following process steps: screen **printing** (**solder** paste), glue ... These include the sequence of component placements on a printed **circuit** board, the allocation ...

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... of **solder** paste rheology with computational simulations of the stencil **printing** ...

R Durairaj, GJ Jackson, NN Ekere, G ... - **Soldering** and Surface ..., 2002 - emeraldinsight.com
 ... paste flows through the apertures, which are aligned precisely with the printed **circuit** board (PCB ... non-Newtonian constitutive **model** for viscosity/shear rate given by the Cross **model** above. ... be argued that the lower pressure generated by the conventional lead **solder** paste (P1 ...

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Planning for printed circuit board assembly: the state-of-the-art review

P Ji, YF Wan - International Journal of Computer Applications in ..., 2001 - Inderscience
 ... In this method, component leads are **soldered** on the surface of the board, rather than being inserted into ... A mathematical **model** was formulated as a cardinality set-covering problem ... Drezner and Nof [16] described a robotic cell for printed **circuit** card **assembly** and identiŹed the ...

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[PDF] •Failure-assessment software for circuit-card assemblies

M Osterman, TJ Stadterman - PROCEEDINGS OF THE ANNUAL ..., 1999 - calce.umd.edu
 ... Stakeholders Process **Soldering**, laminating, plating, etching Failure **Models** Wearout, overstress Test Laboratories eg, Bell Technologies, Lucent Technologies Inputs ... Performance Analysis Cross-talk, time delay, failed **circuit** identification, EM compatibility, radiation resistance ...

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... **mount** technology electronic **assembly** plant: An integrated **model** using **simulation**

S Lambert, G Abdalnour, J Drolet, B Cyr - International Journal of Flexible ..., 2005 - Springer
 ... The demand for automated printed **circuit** board **assembly** continues to increase with the miniaturization ... to improve flexibility and productivity of the SMT line an integrated **model** using **simulation** ... The company's production system, an SMT line, consisted of a **solder** paste **printer** ...

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W Zhiping, N Jingxu - ACTA MECHANICA SINICA (English Series), 2002 - cstam.org.cn
 ... theory and the physical failure mecha- nism, a new MDS methodology, which includes the material constitutive **models**, the MDS ... Hill, 1997 5 Sealing S, Dasgupta A. Alternative accelerated testing method for localization of **solder** fatigue failures on electronic **circuit** cards ...

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TN Tsai, T Yang - Journal of Manufacturing Technology ..., 2005 - emeraldinsight.com
... The efficiency and effectiveness of the proposed BPN **model** can facilitate the reflow oven setup procedure – a procedure that is often time-consuming if undertaken by a trial-and-error approach. ...
Manko, HH (1995), **Soldering** Handbook for Printed **Circuits** and Surface ...
Cited by 3 - Related articles - All 5 versions

SCK Shiu, ECC Tsang, MB Lam, DS Yeung - ... CONFERENCE ON SYSTEMS ..., 1998 - Citeseer
 ... The constructed **model** adopted in this paper was based on a factory's Surface **Mount** Technology
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 pick and place process, error detection and recovery process, **solder** paste re ...
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D Santos, J Kane, F Caballero, K Nagarajan - Computers & Industrial ..., 1995 - Elsevier
... While different types of boards may require different amounts of time in the **solder** paste application ...
At this point, the **simulation model** is completed when inputs are added. ... number of components
per **circuit**, number of **circuits** per board, materials cost per **circuit**, etc.) the program ...
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